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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/683,166	Applicant(s) KODATE ET AL.
	Examiner Leonid Shapiro	Art Unit 2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18,19 and 22* is/are allowed.

6)☒ Claim(s) *1-17,20,21 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings were received and approved on 04-19-04. These drawings are Figs. 27-28.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the newly introduced limitation of claim 4: "first and second pixel electrodes having different electrical characteristics from one another" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The newly introduced limitation of claim 4: "first and second pixel electrodes having different electrical characteristics from one another".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. For the newly introduced limitation of claim 4: "first and second pixel electrodes having different electrical characteristics from one another" it is not clear which different electrical characteristics are different? Is the difference related only to different physical location or any other reasons?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3,14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Libsch et al. (US Patent No. 6,476,787 B1).

As to claim 1, Kwon teaches an image display device, comprising: a plurality of signal lines for supplying a display signals (See Fig. 6A, items D1-Dn, in description See Col. 5, Line 1-24); a plurality of scanning lines for supplying a scanning signals (See Fig. 6A, items G1-Gn, in description See Col. 5, Line 1-24); first and second pixel electrodes to which display signals are supplied from specified one of signal lines (See Fig. 6A, items 71c and 73c, in description See Col. 5, Line 1-24); a

first switching element disposed between the specified one of signal lines and first pixel electrode (See Fig. 6A, item 71a, in description See Col. 5, Line 1-24); a second switching element connected to first switching element (See Fig. 6A, item 71b, in description See Col. 5, Line 1-24); a third switching element connected to the specified one of signal lines, the third switching element being for controlling supply of display signals to second pixel electrode (See Fig. 6A, item 73a, in description See Col. 5, Line 1-24).

Kwon does not show the first switching element having a gate electrode for controlling supply of display signals and a second switching element disposed between gate electrode of first switching element and specified one of scanning lines.

Libsch et al. teaches the first switching element having a gate electrode for controlling supply of display signals (See Fig. 1, item M3, Col. 3, Lines 54-66) and a second switching element disposed between gate electrode of first switching element and specified one of scanning lines (See Fig. 1, items M2, Scan Line A, Col. 3, Lines 54-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 2, Libsch et al. teaches a scanning line having nothing to do (relative to timing in the reference) with drive of the first and second pixel electrodes (See Figs. 5-6, items Scan Lines A, C, D, CS1, CS2, Col. 4, Lines 24-58) is formed, a storage

capacitor is formed between scanning line (See Fig. 5, item C, D) and each first and second pixel electrodes (See Fig. 5, item CS1, CS2, Col. 4, Lines 24-58).

As to claim 3, Libsch et al. teaches a storage capacitor is formed between scanning line (See Fig. 5, item D) and each first and second pixel electrodes (See Fig. 5, item CS1, CS2, Col. 4, Lines 24-58), specified scanning line being disposed at a front stage of first and second pixel electrodes (See Fig. 5, item D).

As to claim 14, Kwon teaches an image display apparatus, which arrays pixels in a matrix fashion composed of M rows and N columns (M and N: arbitrary positive integer) to form an image display section (See Fig. 5A, items D1-Dn, G1-Gn, in description See Col. 3, Lines 59-65), image display apparatus comprising: a signal line driving circuit for supplying display signals (See Fig. 2, item 23, in description See Col. 1, Lines 37-47); a scanning line driving circuit for supplying scanning signals (See Fig. 2, item 22, in description See Col. 1, Lines 37-47); a plurality of signal lines extending from signal line driving circuit (See Fig. 6A, item D1-Dn); a plurality of scanning lines extending from scanning line driving circuit (See Fig. 6A, item G1-Gn); a first switching element driven by a scanning signal from a second scanning line, the first switching element being for controlling supply of a display signal from specified signal line to first pixel electrode (See Fig. 6A, item 71a, in description See Col. 5, Lines 1-24); a second switching element driven by a scanning signal from first scanning line (See Fig. 6A, item 71b, in description See Col. 5, Lines 1-24); a third switching element driven by a scanning signal from first scanning line, the third switching element being for contr4olling supply of display signal from specified signal line to second pixel electrode

(See Fig. 6A, item 73a, in description See Col. 5, Lines 1-24 and Col. 4, Lines 27-28); the first and second pixel electrodes arranged (See Fig. 6A, items 71c, 73c. Col. 5, Lines 1-24 and Col. 4, Lines 1-3) between a n-th scanning line and (n+1)-th scanning line and are adjacent to each other (See Fig. 6A, items G1,G2, Col. 5, Lines 1-24) with specified signal line interposed therebetween (See Fig. item D1, Col. 5, Lines 1-24 Col. 3, Lines 59-65).

Kwon does not show the second switching element being for controlling turning ON/OFF of first switching element.

Libsch et al. teaches the second switching element (See Fig. 1, item M2, Col. 3, Lines 54-66) being for controlling turning ON/OFF of first switching element (See Fig. 1, items M3, Col. 3, Lines 54-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 15, Libsch et al. teaches a fourth switching element driven by the scanning signal from the from (n+2) scanning line (See Fig. 3, items M1, Scan Line C, Col. 4, Lines 4-16), the fourth switching element being for controlling turning ON/OFF of third switching element (See Fig. 3, items M1, M2, Col. 4, Lines 4-16).

6. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Yamahara et al. (US Patent No. 5,579,140).

As best understood by examiner, Kwon teaches an image display device (See Col. 1, Lines 6-13), comprising: a signal line for supplying a display signal (See Fig. 6A, item D1, in description See Col. 5, Line 1-24); first and second pixel electrodes (See Fig. 5A, items 71c and 73c, from Col. 3, Line 65 to Col. 4, Line 5) arranged in a checked pattern so as interpose signal line therebetween (See Fig. 6A, items 71c and 73c, in description See Col. 5, Line 1-24); a first switching element connected to signal line, the first switching element being for controlling supply of display signal to first pixel electrode (See Fig. 6A, item 71a, in description See Col. 5, Line 1-24); a second switching element connected to first switching element (See Fig. 6A, item 71b, in description See Col. 5, Line 1-24); a third switching element connected to signal line, the third switching element being for controlling supply of display signals to second pixel electrode (See Fig. 6A, item 73a, in description See Col. 5, Line 1-24); a first scanning line for supplying a scanning signal to second and third switching elements (See Fig. 6A, item G1, in description See Col. 5, Line 1-24); a second scanning line for supplying a scanning signal to first switching element (See Fig. 6A, item G2, in description See Col. 5, Line 1-24).

Kwon does not show first and second pixel electrodes having different electrical characteristics from one another.

Yamahara et al. teaches first and second pixel electrodes having different electrical characteristics from one another (See Col. 2, Lines 55-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Yamahara et al. into the Kwon apparatus in order to widen the range of applications.

7. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon and Yamahara et al. as applied to claim 4 above, and further in view of Libsch et al.

As to claim 5, Kwon and Yamahara et al. do not show first scanning line is disposed at a rear stage of the first and second pixel electrodes, and second scanning line disposed at rear stage of the first scanning line.

Libsch et al. teaches first scanning line is disposed at a rear stage of the first and second pixel electrodes (See Fig. 5, item Scan Line D, Col. 4, Lines 17-23) and second scanning line disposed at rear stage of the first scanning line (See Fig. 3, item Scan Line C, Lines 17-23).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 6, Kwon and Yamahara et al. do not show a third scanning line at a front stage of first and second pixel electrodes, and a storage capacitor is formed between third scanning line and each first and second electrodes.

Libsch et al. teaches a storage capacitor is formed between scanning line (See Fig. 5, item D) and each first and second pixel electrodes (See Fig. 5, item CS1, CS2,

Col. 4, Lines 24-58), specified scanning line being disposed at a front stage of first and second pixel electrodes (See Fig. 5, item D).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 7, Kwon and Yamahara et al. do not show first switching element directly connects first pixel electrode and signal line.

Libsch et al. teaches first switching element directly connects first pixel electrode and signal line (See Fig. 5, items M3, CS1, Col. 4, Lines 24-58).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 8, Kwon and Yamahara et al. do not show first scanning line is arranged at a front stage of the first and second pixel electrodes, and a scanning line is arranged at a rear stage of the first and second electrode.

Libsch et al. teaches first scanning line is disposed at a rear stage of the first and second pixel electrodes (See Fig. 5, item Scan Line D, Col. 4, Lines 17-23) and second scanning line disposed at rear stage of the first scanning line (See Fig. 3, item Scan Line C, Lines 17-23).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 9, Kwon and Yamahara et al. do not show a fourth switching element connected to third switching element, the forth switching element being supplied with a scanning signal from second scanning line.

Libsch et al. teaches fourth switching element connected to third switching element (See Fig. 3, item M1, Col. 4, Lines 4-16), the forth switching element being supplied with a scanning signal from second scanning line (See Fig. 3, items M1, Scan line C, Col. 4, Lines 4-16).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiyoshi et al. (US Patent No. 6,323,871 B1) in view of Kwon.

Fujiyoshi et al. teaches an image display apparatus, which arrays pixels in matrix fashion composed of M rows and N columns M and N: arbitrary positive integer) to form an image display section (see fig. 2, items G1-G4, S1-S2, in description See Col. 5, lines 22-35), image display apparatus comprising: a signal driving circuit for

supplying display signals (See Fig. 1, item Sd, in description See Col. 5, Lines 5-15); a scanning line driving circuit for supplying scanning signals (See Fig. 1, item Gd, in description See Col. 5, Lines 5-15); a plurality of signal lines extending from signal line driving circuit (See Figs.1-2, items S1-S2, in description See Col. 5, Lines 5-35); a plurality of scanning lines extending from scanning line driving circuit (See Figs.1-2, items G1-G4, in description See Col. 5, Lines 5-35); and first, second and third electrodes arrayed on the same display line, the first, second and third electrodes being supplied with display signals from a specified signal line (See Fig. 2, items S1. 11, in description See Col. 5, Lines 22-35 and col. 7, Lines 33-40); wherein first, second and third pixel electrodes are driven by scanning signals from different scanning lines (See Fig. 2, items G1-G3, in description See Col. 5, Lines 22-35).

Fujiyoshi et al. does not show first, second and third pixel electrodes connected to a the same signal line and arrayed on the same display line in parallel with a scanning line.

Kwon teaches first, second and third pixel electrodes connected to a the same signal line and arrayed on the same display line in parallel with a scanning line (See Fig. 6A, items 71c and 73c, in description See Col. 5, Line 1-24).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Kwon in the Fujiyoshi et al. apparatus in order to be able to display images with the same resolution while its data lines are as many as half the number of the data lines of the conventional one (See Col. 2, Lines 25-19 in the Kwon reference).

9. Claims 10-13, 16-17, 21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Libsch et al.

As to claim 10, Kwon teaches an image display device, in which a plurality of signal lines for supplying display signals and plurality of scanning lines for supplying scanning signals are arrayed in a matrix fashion (See Fig. 5A, items D1-Dn, G1-Gn, in description See Col. 3, Lines 59-65), comprising the first and second pixel electrodes arranged between a n-th scanning line and a (n+1)-th scanning line (n: positive integer) (See Fig. 5A, items G1, G2, 71c, 73c, Col. 4, Line 6-28), the first and second pixel electrodes being supplied with a display signal from a specified signal line (See Fig. 5A, items 71c and 73c, in description See Col. 3, Lines 59-65); a first switching mechanism for permitting the display signal pass therethrough when first scanning line and second scanning line are simultaneously being selected (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58); and a second switching mechanism for permitting the display signal to pass through to second pixel electrode when first scanning line is being selected (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58).

Kwon does not show a storage capacitor is formed between each of first and second pixel electrodes and n-scanning line.

Libsch et al. teaches a storage capacitor is formed between each of first and second pixel electrodes and n-th scanning line (See Fig. 8, item CS1, CS3, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claims 11, Kwon teaches a third pixel element arranged between n-th scanning line and n+1 scanning line (N: positive integer) (See Fig. 5A, items G1, G2, G3..., Col. 3, from Col. 3, Line 59 to Col. 4, Line 5).

As to claim 12, Kwon teaches a first switching mechanism includes: a first switching element connected to specified signal line, the first switching element being driven by a scanning signal supplied from (n+10th scanning line (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58); and a second switching mechanism connected to first switching element being driven by a scanning signal supplied from (n+m)-th scanning line (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58).

As to claim 13, Kwon teaches an image display device, in which a plurality of signal lines for supplying display signals and plurality of scanning lines for supplying scanning signals (See Fig. 5A, items D1-Dn, G1-Gn, in description See Col. 3, Lines 59-65), the first pixel electrode arranged between a n-th scanning line and a (n+1)-th scanning line (n: positive integer) (See Fig. 5A, items G1, G2, 71c, 73c, Col. 4, Line 6-28); the first and second pixel electrodes connected to a specified signal line (See Fig. 5A, items 71c and 73c, in description See Col. 3, Lines 59-65); wherein first pixel electrode is driven by a first scanning signal from first scanning line and by a second

scanning signal from a second scanning line (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58); and a second pixel electrode is driven by a scanning signal from first scanning line (See Fig. 5B, items a and b, in description See Col. 4, Lines 37-58).

Kwon does not show a storage capacitor disposed between first pixel electrode and n-scanning line.

Libsch et al. teaches a storage capacitor disposed between each of pixel electrode and n-th scanning line (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 16, Kwon teaches an image display apparatus, which arrays pixels in a matrix fashion composed of M rows and N columns (M and N: arbitrary positive integer) to form an image display section (See Fig. 5A, items D1-Dn, G1-Gn, in description See Col. 3, Lines 59-65), image display apparatus comprising: a signal line driving circuit for supplying display signals (See Fig. 2, item 23, in description See Col. 1, Lines 37-47); a scanning line driving circuit for supplying scanning signals (See Fig. 2, item 22, in description See Col. 1, Lines 37-47); a plurality of signal lines extending from signal line driving circuit (See Fig. 6A, item D1-Dn); a plurality of scanning lines extending from scanning line driving circuit (See Fig. 6A, item G1-Gn); the first and

second pixel electrodes arranged between a n-th scanning line and a (n+1)-th scanning line (n: positive integer) and are adjacent to each other with specified signal line interposed therebetween (See Fig. 5A, items G1, G2, D1, 71c, 73c, Col. 4, Line 6-28); a first switching element driven by a scanning signal from a second scanning line, the first switching element being for controlling supply of a display signal from specified signal line to first pixel electrode (See Fig. 6A, item 71a, in description See Col. 5, Lines 1-24); a second switching element driven by a scanning signal from first scanning line (See Fig. 6A, item 71b, in description See Col. 5, Lines 1-24); a third switching element driven by a scanning signal from first scanning line, the third switching element being for contr4olling supply of display signal from specified signal line to second pixel electrode (See Fig. 6A, item 73a, in description See Col. 5, Lines 1-24 and Col. 4, Lines 27-28).

Kwon does not show a storage capacitor is formed between each of first and second pixel electrodes and n-scanning line.

Libsch et al. teaches a storage capacitor disposed between each of pixel electrode and n-th scanning line (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 17, Libsch et al. teaches a storage capacitor disposed between each of pixel electrode and n-th scanning line (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

As to claim 21, Kwon teaches an image display apparatus, which arrays pixels in a matrix fashion composed of M rows and N columns (M and N: arbitrary positive integer) to form an image display section (See Fig. 5A, items D1-Dn, G1-Gn, in description See Col. 3, Lines 59-65), image display apparatus comprising: a signal line driving circuit for supplying display signals (See Fig. 2, item 23, in description See Col. 1, Lines 37-47); a scanning line driving circuit for supplying scanning signals (See Fig. 2, item 22, in description See Col. 1, Lines 37-47); a plurality of signal lines extending from signal line driving circuit (See Fig. 6A, item D1-Dn); a plurality of scanning lines extending from scanning line driving circuit (See Fig. 6A, item G1-Gn); the first and second pixel electrodes arranged between a n-th scanning line and a (n+1)-th scanning line (n: positive integer) and are adjacent to each other with specified signal line interposed therebetween (See Fig. 5A, items G1, G2, D1, 71c, 73c, Col. 4, Line 6-28); a first switching element driven by a scanning signal from a second scanning line, the first switching element being for controlling supply of a display signal from specified signal line to first pixel electrode (See Fig. 6A, item 71a, in description See Col. 5, Lines 1-24); a second switching element driven by a scanning signal from first scanning line (See Fig. 6A, item 71b, in description See Col. 5, Lines 1-24); a third switching element driven by a scanning signal from first scanning line, the third switching element being for

contr4olling supply of display signal from specified signal line to second pixel electrode (See Fig. 6A, item 73a, in description See Col. 5, Lines 1-24 and Col. 4, Lines 27-28).

Kwon does not show the second switching element being for controlling turning ON/OFF of first switching element.

Libsch et al. teaches the second switching element (See Fig. 1, item M2, Col. 3, Lines 54-66) being for controlling turning ON/OFF of first switching element (See Fig. 1, items M3, Col. 3, Lines 54-66).

As to claim 23, Kwon teaches an image display apparatus, comprising a plurality of signal lines for supplying display signals (See Fig. 6A, item D1-Dn); a plurality of scanning lines for supplying scanning signals (See Fig. 6A, item G1-Gn); a pixel electrode supplied with a display signal from specified signal line (See Fig. 6A, item 71c, in description See Col. 5, Lines 1-24); a first switching element connected to pixel electrode (See Fig. 6A, item 71b, in description See Col. 5, Lines 1-24).

Kwon does not show a second switching element for controlling turning ON/OFF of the first switching element and a storage capacitor arranged between pixel electrode and one of scanning lines adjacent to pixel electrode and a storage capacitor arranged between pixel electrode and n- scanning line.

Libsch et al. teaches the second switching element (See Fig. 1, item M2, Col. 3, Lines 54-66) being for controlling turning ON/OFF of first switching element (See Fig. 1, items M3, Col. 3, Lines 54-66) and a storage capacitor arranged between pixel electrode and n-scanning line (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 24, Kwon teaches an image display apparatus, comprising a plurality of signal lines for supplying display signals (See Fig. 6A, item D1-Dn); a plurality of scanning lines for supplying scanning signals (See Fig. 6A, item G1-Gn); a pixel electrode supplied with a display signal from specified signal line (See Fig. 6A, item 71c, in description See Col. 5, Lines 1-24); a first switching element connected to pixel electrode (See Fig. 6A, item 71b, in description See Col. 5, Lines 1-24); wherein pixel electrode is driven by scanning signals supplied from at least two scanning lines excluding the one of scanning lines (See Fig. 6A, items 71a, 73a, in description See Col. 5, Lines 1-24);

Kwon does not show a storage capacitor arranged between pixel electrode and one of scanning lines adjacent to pixel electrode.

Libsch et al. teaches a storage capacitor arranged between pixel electrode and one of scanning line adjacent to pixel electrode (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

As to claim 25, Kwon teaches a method of driving an image display device which comprises: a plurality of signal lines for supplying display signals (See Fig. 6A, item D1-Dn); a plurality of scanning lines for supplying scanning signals (See Fig. 6A, item G1-Gn); the first pixel electrode arranged between a n-th scanning line and a (n+1)-th scanning line (n: arbitrary positive integer) (See Fig. 5A, items G1, G2, D1, 71c, 73c, Col. 4, Line 6-28); the first pixel electrode being connected to a specified signal line; and a second pixel electrode being connected to a specified signal line (See Fig. 6A, items 71c and 73c), the method comprising steps of: supplying a first display signal to specified signal line, the first display signal having a first potential to be given to first pixel electrode, for a period from the time when potentials of first scanning line and second scanning line become equal to a selection potential to the time when the potential of first scanning line becomes equal to a non-selection potential, thus giving first potential to first and second pixel electrodes (See Fig. 6B, item a, in description See Col. 4, Lines 37-67 and Col. 5, Lines 16-24); and supplying a second display signal to specified signal line, the second display signal having a second potential to be given to second pixel electrode, after the potential of first scanning line and second scanning line becomes equal to the non-selection potential, thus giving second potential to second pixel electrode (See Fig. 6B, item b, in description See Col. 4, Lines 37-67 and Col. 5, Lines 16-24).

Kwon does not show a storage capacitor disposed between first pixel electrode and n-scanning line.

Libsch et al. teaches a storage capacitor arranged between pixel electrode and n-scanning line (See Fig. 8, item CS1, Scan Line D, Col. 5, Lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of invention to use configuration as shown by Libsch et al. in the Kwon and Yamahara et al. apparatus in order to reduce number of gate and data drivers to reduce costs (See Col. 1, Lines 38-40 in the Libsch et al. reference).

Response to Amendment

11. Applicant's arguments filed on 04-19-04 with respect to claim 1-17, 20-21, 23-25 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

12. Claims 18-19, 22 are allowed.

13. Relative to independent claims 18-19, 22 the major difference between the teaching of the prior art of record (US Patent No. 6,512,504 B1, Yamauchi et al. and US Patent No. 6,486,930 B1, Kwon) and the instant invention is that the said prior art **does not teach** one signal line are supplying three pixel electrodes with image signals and the control circuit with five switching elements.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Ls 06.17.04

VIJAY SHANKAR
PRIMARY EXAMINER